CHAOTIC BEHAVIOUR EVALUATION IN OPTICAL LOGIC GATES WITH FRACTAL CONCEPTS

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ABSTRACT

A chaotic output was obtained previously by us, from an Optical Programmable Logic Cell when a feedback is added. Some time delay is given to the feedback in order to obtain the non-linear behaviour. The working conditions of such a cell is obtained from a simple diagram with fractal properties. We analyze its properties as well as the influence of time delay on the characteristics of the working diagram. A further study of the chaotic obtained signal is presented.

Keywords: fractal, digital chaos, optical logic gates

1. INTRODUCTION

It is well accepted nowadays that many geometric objects in the natural and technical world have fractal-like shapes and surfaces. This fractal structure has been studied in many cases just as a geometrical curiosity with some implications in the field where it has been observed. In some others, it has been analysed due to the possible implications it has with the non-linear behaviours existing at some particular system. This last aspect is the one will be studied in this paper. It concerns the connection between the chaotic signal obtained from an optical logic gate and the resulting phase diagrams.

The analysis of chaotic structures has been the object of a large number of papers in the last years. Most of them are related with behaviour derived from the implementation of some set of partial differential equations at a particular system. In many cases, this system was an electronic set-up with controlling equations the same set of equations analysed previously from a mathematical point of view. Chua's circuits are one of the most well known studied cases. In any of them, derived from the starting point, signals were analogic. This fact allows the use of a standard mathematical analysis.

But the above situation is no longer valid when the system is digital by nature and the output has a digital character too. The type of analysis previously employed in analogic systems may be not directly applied here. For instance, an straightforward method to study chaos, the phase diagram, is not possible to apply here. If one has just two possible outputs, a "1" and a "0", the phase diagram of this system should be composed by four points only. And this diagram should give no information about the properties of such a system. If this is the case for a simple situation as the phase diagram other employed methods in analogic chaos would have similar problems. This is the reason why some other techniques need to be implemented when one is dealing with digital signals.

A digital chaotic system has been reported by us in several places[1-6]. Its properties have been analyzed by numerical techniques and some conclusions have been obtained. But a particular aspect of this system has not been studied yet. It is related with the fractal-like properties that appear when its digital behaviour is represented in a working diagram. Because it is not possible, by now, to determinate a set of equations that give indication about its way of working, a peculiar logic diagram was presented. It offer the possibility to know what type of logic function is performed depending on the type of applied control signal and the level of signals. The important point of this working diagram is that offers a fractal like structure depending its properties on the precision adopted in the computer simulation. Because this fractal line indicates the boundary contour between the different logic operations performed by the cell, its structure will be related with the jumps between regions and hence with its behaviour. If the optical logic cell operates under strict logic conditions, that is to say, working for example as a part of an optical computer, the fractal properties of the boundary between regions will affect to the precision of the performed logic function. But if it is working under a chaotic regime, the chaotic output will have some relation with the above mentioned fractal structure. The main objective of this paper will be to analyze some of the possible indicated relations between the fractal structure and the chaotic regime.

The paper will be divided into two main parts. The first one will be just a short summary of the main properties of the optical logical cell. Although most of them have been reported previously, it is necessary to review some of them because they will be necessary for the further study. The second one will present the properties derived from some changes in the parameters of the cell and its simulation and how this changes affect to the chaotic properties. The relation with the existing fractal structure at the working diagram will be presented.

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2. OPTICAL LOGIC CELL

The optical logic cell we have studied is based in two principal devices. The first one is a simple "On-Off" device that can be easily be implemented by a common OLE (Optical Logic Etalon). The second one corresponds to a more complicated device with non-linear characteristics. It can represented by a conventional SEED (Self Electro-optic Effect Device). The way these two devices are connect inside our OPLC (Optically Programmable Logic Cell) can be seen in Fig. 1. The inset indicates the type of device is inside each block.

The OPLC has two digital signal data inputs (I_1, I_2) and two digital signals data outputs (O_1, O_2). Two other inputs allow the addition of control signals (h, g). They allows to determinate which one of the eight possible Boolean functions (ON, OFF, AND, OR, XOR, NAND, NOR, XNOR) is going to be implemented the cell and obtained at output O_1. Output O_2 allows just four different types of functions ON, AND, OR and OFF. This cell was initially designed for optical computing. An extensive analysis can be found on [1]. Only the results more directly related with the present objective of this paper will be reproduced here.

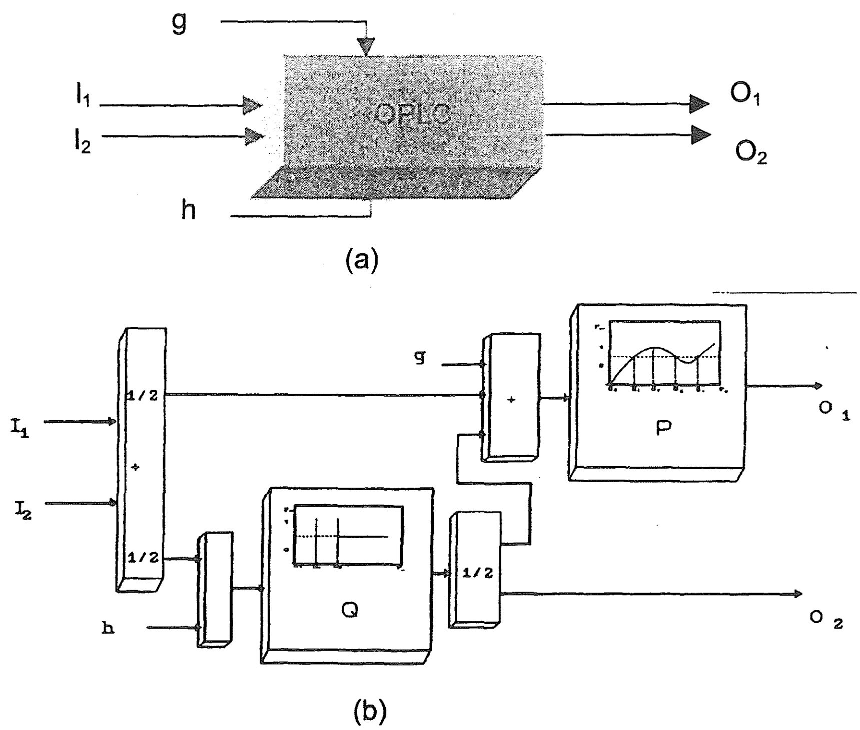


Figure 1.- Block Diagram of the OPLC –Optically Programmable Logic Cell **(a)** External. **(b)** Internal.

The simulation of the OPLC has been done with Simulink. Fig. 2 shows the block diagram model employed in this program.

Although input and output data signals are binary, the internal cell processing is a multilevel process. Because this cell is intended to work with optical signals, it is straightforward to handle these multilevel signals. Just an optical coupler can perform the addition of the different signals. These couplers are indicated in our present simulation by blocks.

A further point needs now to be clarified. As it was pointed out before, the output is digital. But the processing signal depends mainly in the position of the decision level. Moreover, there is a certain hysteresis loop in anyone of the employed processing elements, in relation with the signal level of the binary data input. This hysteresis is due to several facts that will be commented later.

The versatility of this cell is due mainly to the P device behaviour. Hence, so we must pay more attention to it. The real SEED characteristics have been adapted to a more convenient form. Our simulation allows to this device just two output values, namely "1" and "0". This allows us the processing of multilevel input signals, giving a binary output with these two signal levels. This ideal characteristic is easy to simulate by computer with ample freedom in changing the values of the internal parameters, such as decision level and its hysteresis. An analog implementation with an optoelectronic model is also possible and was partially done by us[2]. To employ digital electronic is more complicated as well as an all- optical implementation with the SEED device. This last device has small tolerance and is no easy to duplicate is behaviour. It is because that in this paper we have restricted our work to a computer simulation.

In order to characterise the cell behaviour, we have made the representations shown in Fig. 3. It represents the output O_1, where the decision level normalised to a bit "1" of the input data appears on x-axis and the different levels that control signal g can adopt, on y-axis.

As it can be seen in Fig. 1(b), the output O_1, which correspond to the output of device P, depends on the output of device Q as well as on the control signal g . This indicates that there should be different results to the shown in figure 3, for the different Q-device outputs. In the present case, we will just consider the case for one of the possible outputs of the Q-device. We will extrapolate the analysis to the rest of the cases. The representation of P-device output, shown in figure 3, corresponds to an AND function on Q-device output O_2.

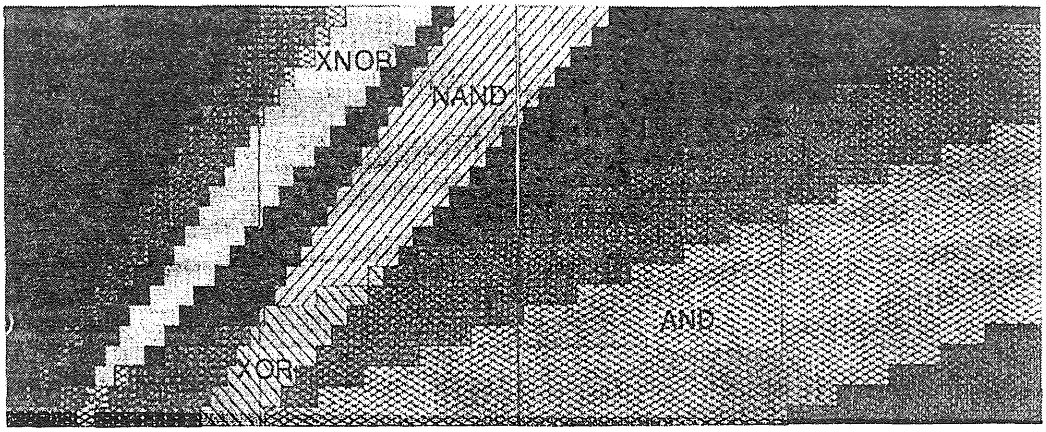
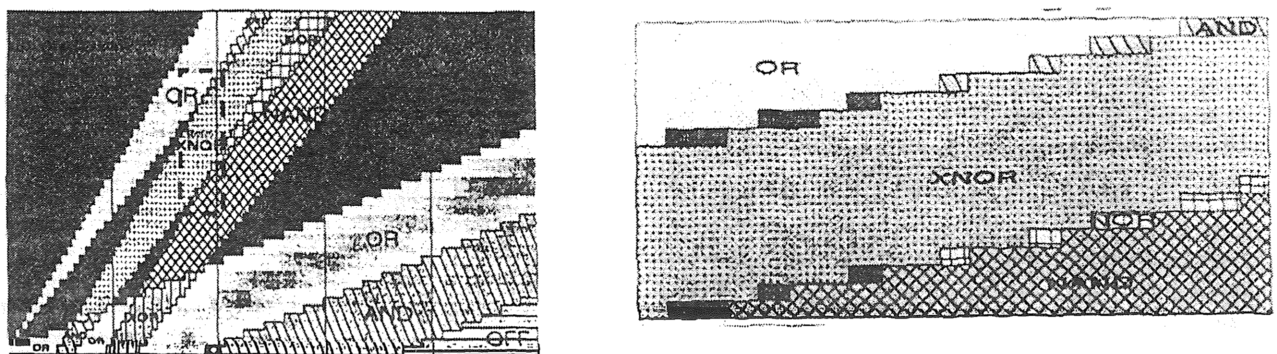


Figure 3.- Output O_2 characteristic with output O_1 = AND.

3. FRACTAL CHARACTERISTICS

The geometric pattern of figure 3 shows different areas corresponding to the different Boolean logic function the OPLC is able to perform. As it can be seen, the boundaries are step-like. If we try to measure the total area for a particular logical function the task is not straightforward. This is because there is not a clear mathematical function defining the cell behaviour. This is due to the discrete character of the functions involved in the process. Moreover, it is difficult too because there always exists a certain hysteresis in any real device depending on the type and characteristics of its fabrication. So we can say that this geometric figure is similar to the problem of coast length evaluation that give us a different length depending on the scale to measure it that we use.

The first concept of a fractal structure is the concept of self similarity. A structure is said to be self-similar if it can be broken down into arbitrarily small pieces, each of which is a small replica of the entire structure[9]. In this sense, we have study the work diagram of device P, that is represented on Fig. 4.a. In order to simplified the analysis we take the small portion marked and represented on Fig.4.b. As it is indicated, the scale in this figure corresponds to a precision of decimals on the control signal (y-axis) and of hundredths on the decision level (x-axis). The variation of decision level can be interpreted as a variation on the level signal of a bit "1" input data.



(a)

(b)

Figure 4.-a) P-device output characteristic with a variation of controls signal =0.1 and of decision level = 0.01.**b)** detail marked on a)

If we modified the precision scale of both axis we obtain similar structures. Some examples of this structure are show in Fig. 5.a, 5.b, and 5.c. So far, we can say that working diagram of P-device has a self-similarity property, but we can not say that it is also a fractal. We must analyze the fractal dimension[9]. As it is well known, there are several methods to calculate fractal dimension and among them, box-counting dimension is the one with more applications in science. The

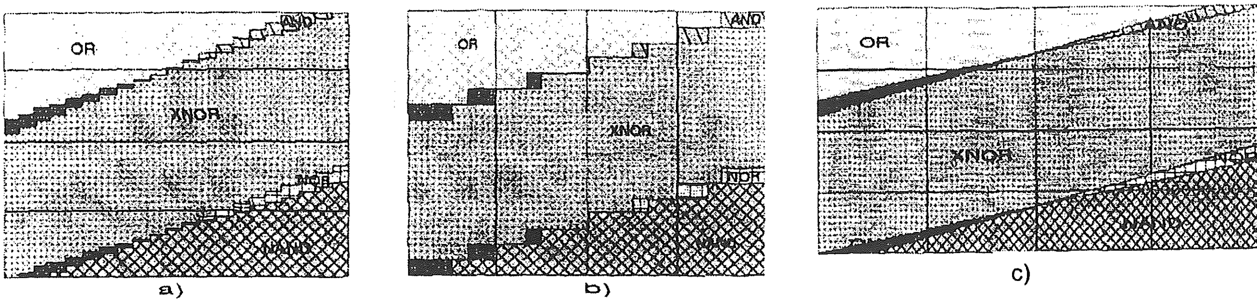


Figure 5.- Different scale representation of fig.5.b **a)** controls signal =0.01 and of decision level = 0.01, **b)** controls signal =0.1 and of decision level = 0.001, **c)** controls signal =0.01 and of decision level = 0.001.

reason to this is the simplicity of its calculation. Table 1 is the resume of box-counting dimension and self-similarity dimension for structures of figure 5. As it can be seen, the dimension is always fractional. This result allows us to believe that that the structure of the P-device working diagram is a fractal and hence it must have fractal characteristics.

S	u	d	k	$D_{k+1,k}$
0.01/0.001	554	0.9145	1	$D_{2,1} = 0.98$
0.01/0.01	58	0.8817	2	$D_{2,1} = 0.91$
0.1/0.01	7	0.8451	3	

Table 1.- Resume of fractal dimension of figure 5 structures.

d = self-similarity dimension

$D_{k+1,k}$ = box-counting dimension

4. TOLERANCE EVALUATION

The fractional value of fractal dimension can give us some information about the tolerance in the control signal and in the data signal in order to obtain the logical Boolean function expected at the output of the device. We can observe that at higher precision the self-similarity dimension is closer to one. So, the variation of the input data from 0,001 to 0,002 is much least critical than in the case of going from 0,01 to 0,02. At the same time, the box-counting dimension obtained from structure k=1 and k=2 is closer to 1 than the dimension obtained from k=2 and k=3. This gives us the information about how similar is the working diagram between the two structures being compared. This means, for example, than structure k=2 is more similar to structure k=1 than to k=3.

This way of tolerance evaluation is not so easy. Hence we propose here a diagram, equivalent to a phase diagram, of the dynamical system as a method to evaluate the tolerance of a device on its general behaviour. In this case we will pay attention only to the control signal. This will do easier a rapid understanding of our evaluation. The result has been obtained from the Simulinkth simulation model show in Fig. 6.

The pattern of the sum input signal corresponds to a [2 1 1 0]. If we evaluate with this pattern, every four output bits, we can know which Boolean function is performed. If we represent these four bits in an hexadecimal format[1], we can relate every hexadecimal digit with a Boolean function as it is written on Fig. 7. The right column of plots in figure 7 corresponds to the different functions that can be obtained from two trains of input data signal changing on time the level of the control signal g (see Fig. 1) with the precision indicated in each case. The left column of plots show the phase diagram of output in instants t and t+1, obtained with the hexadecimal representation. This way of representing the behaviour of the system that gives us more information than the digital one[2].

As we can observe the phase diagram is changing with the level of precision. A precision higher than 0,001, as far as we have evaluated the system, seams to give the same behaviour. So the level of

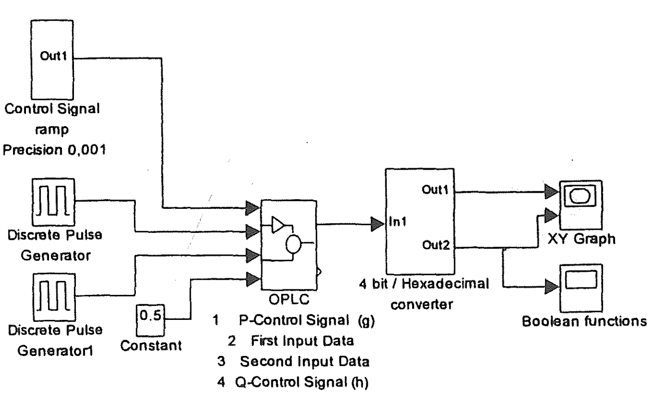
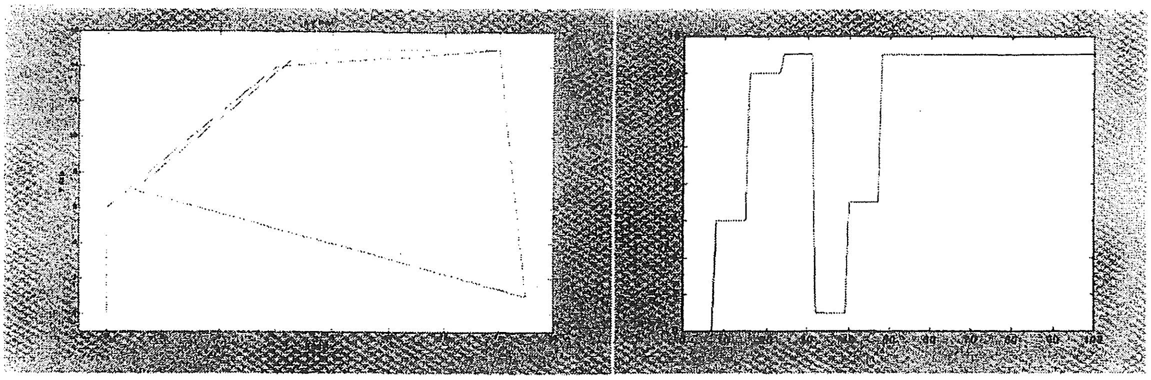


Figure 6.- Simulinkth Block Diagram model.

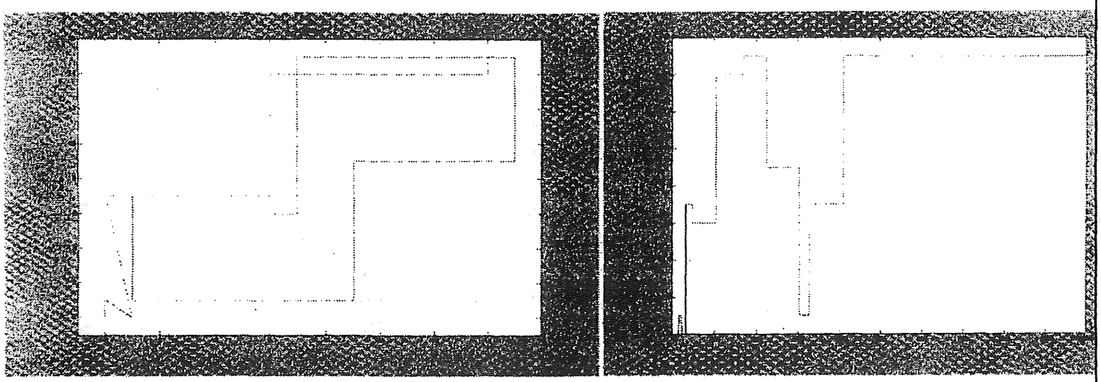
tolerance it would be at thousandth for the control signal level in order to be employ the device as expected.

The result obtained, for the case of thousandth precision, on output O_2 it has a time evolution of 1-7-6-14-15-9-1-7-15 which correspond with the logical function: AND-XOR-OR-NAND-ON-XNOR-OR-ON. If we look on the working diagram of figure 3 we can find a position on x-axis where if we change the control signal level we can see exactly the same evolution. The control signal range, in this case, is larger than the one represented on the working diagram. The different time instant for transition to a new function is not the same on each simulation. This is due to the way the control signal on the simulation has been generated. The ramp slope is smaller at a higher precision. Hence it takes longer to reach the level of the control signal that produces the transition to another type of output.

Control signal = [0 0.1 0.2 0.3 .....]



Control signal = [0 0.01 0.02 0.03 .....]



0 = OFF
1 = AND
6 = XOR
7 = OR
8 = NOR
9 = XNOR
14 = NAND
15 = ON

Control signal = [0 0.001 0.002 0.003 .....]

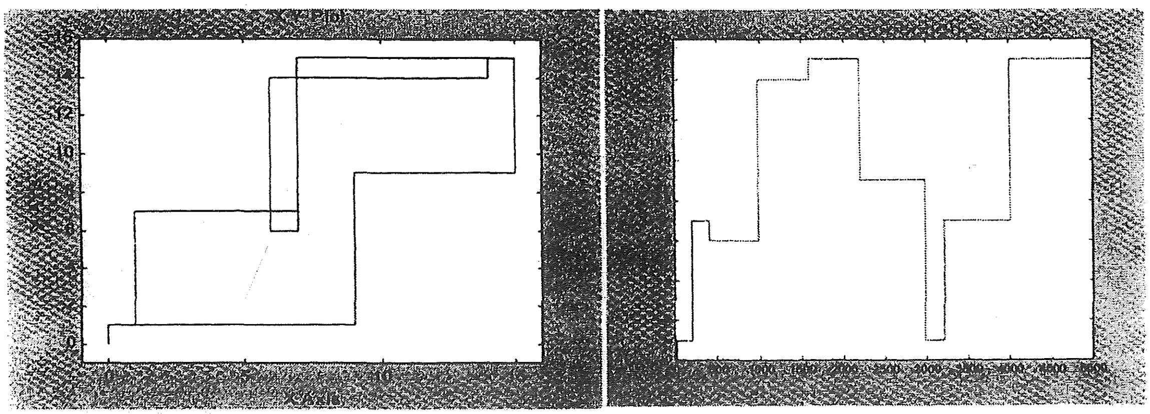


Figure 7.- Hexadecimal code for Boolean function in output O_2. Left column plots are Phase Diagrams (t, t+1). Right column plots are O_2 evolutions in time with the precision level indicated in each case.

5. CHAOTIC BEHAVIOUR

As it has been shown in the literature, the dynamics of non-linear systems depends strongly on the type of delay is added to it. This problem was first analyzed for optical bistable devices, mainly for the case of hybrid systems, when a finite feedback delay comparable to or greater than the combined time constants of all system components is added. The mathematical analysis was made by difference-differential equations because the behaviour was analogic. Ikeda was the first ton apply this type of analysis to a ring cavity system with a nonlinear medium. He concluded that new types of instabilities should be found in such system yielding periodic and chaotic solutions. The main result obtained is that the nonlinear solution depends on the ratio between external time delay and internal time response. When this ratio (external time over internal time) is much larger than one, a highly nonlinear dynamics is achieved. This means than when external time is larger than one order of magnitude than the internal time the situation originates, under certain conditions, a chaotic solution. This problem has been largely studied since the beginning of eighties[7,8].

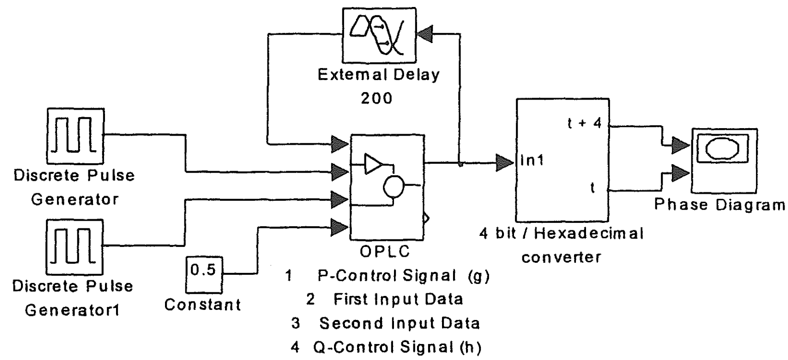


Figure 8.- Optically-Processing Element with feedback

In our present simulation model the internal delay, corresponding to response times of components, has been represented with a similar block as the external delay show in fig. 8. This delay block allows the user to change the delay value.

Before applied the feedback lets analyse the cell behaviour with different internal delay times and with a precision level over thousandth, as the same way as in fig. 6. It was expected to obtain the same phase diagram as in figure 7 with control signal precision of 0.001. Instant of this we find a depended of output behaviour on the internal delay time. In figure 9 are showed some of the results. This result seems to have some kind of dependent with the hexadecimal representation chosen. A deeper analysis must to be done.

In order to obtain chaos we have applied an external delay of 200 and a sum input data with a period equal to 14. On figure 10 it is represented the digital chaotic output, where it seems there is no periodic pattern. The phase diagram obtained for different external delay time is show in figure 11, with a time simulation over 30.0000. Figure 12 show the same time simulation on the conditions to obtain the digital chaos signal. A deeper study of this signal in order to be sure that it is not a random signal but a deterministic one has

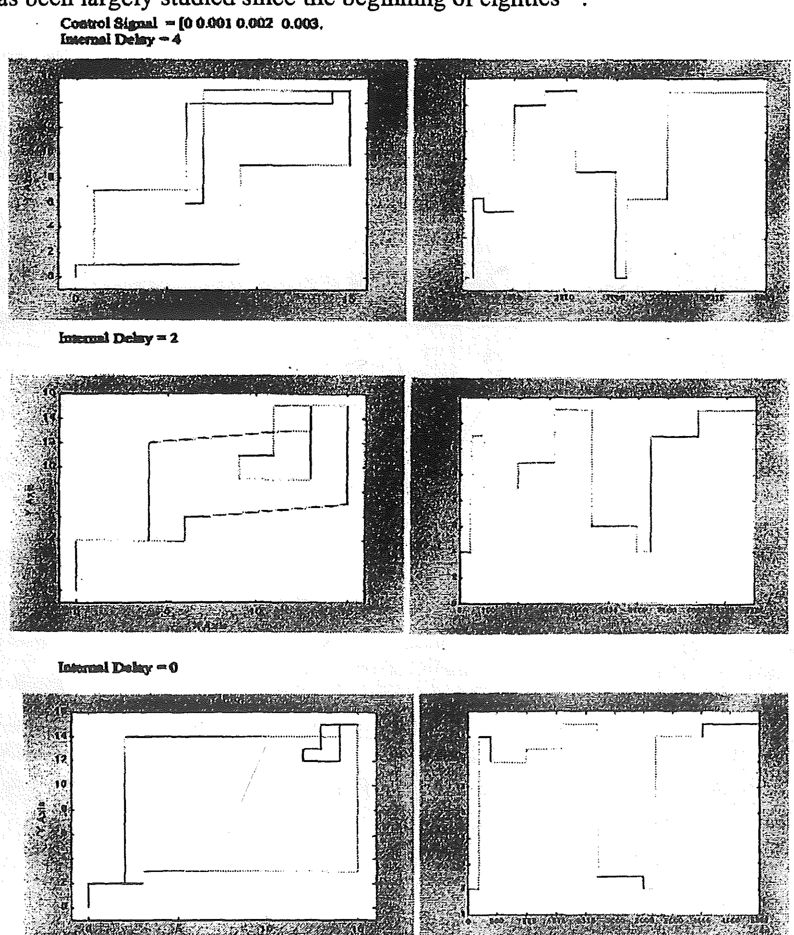


Figure 9.- Hexadecimal code for Boolean function in output O_2. Left column plots are Phase Diagrams (t, t+1). Right column plots are O_2 evolutions in time with the precision level=0.001 and delay time indicated in each

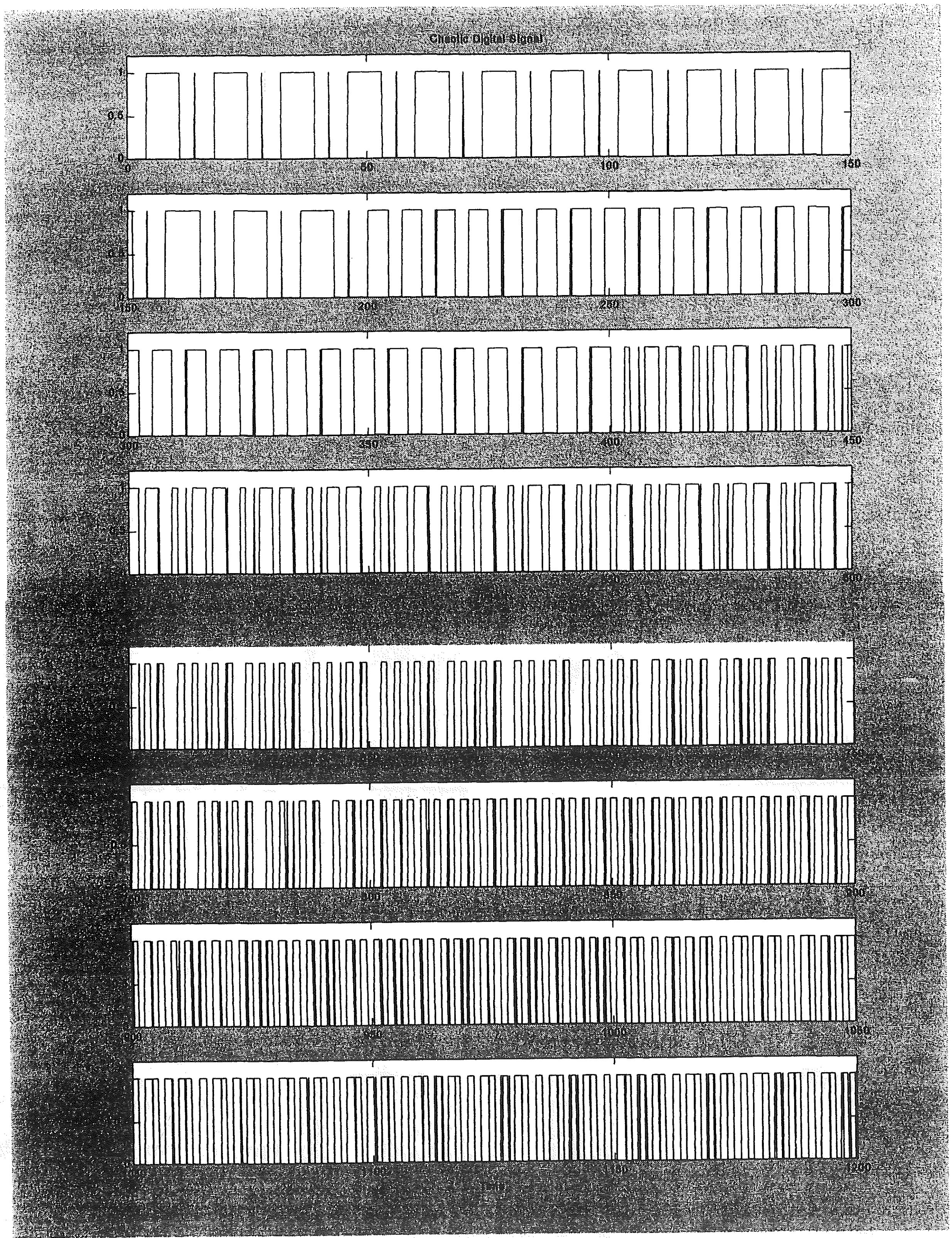


Figure 10.- Digital Chaos Signal.

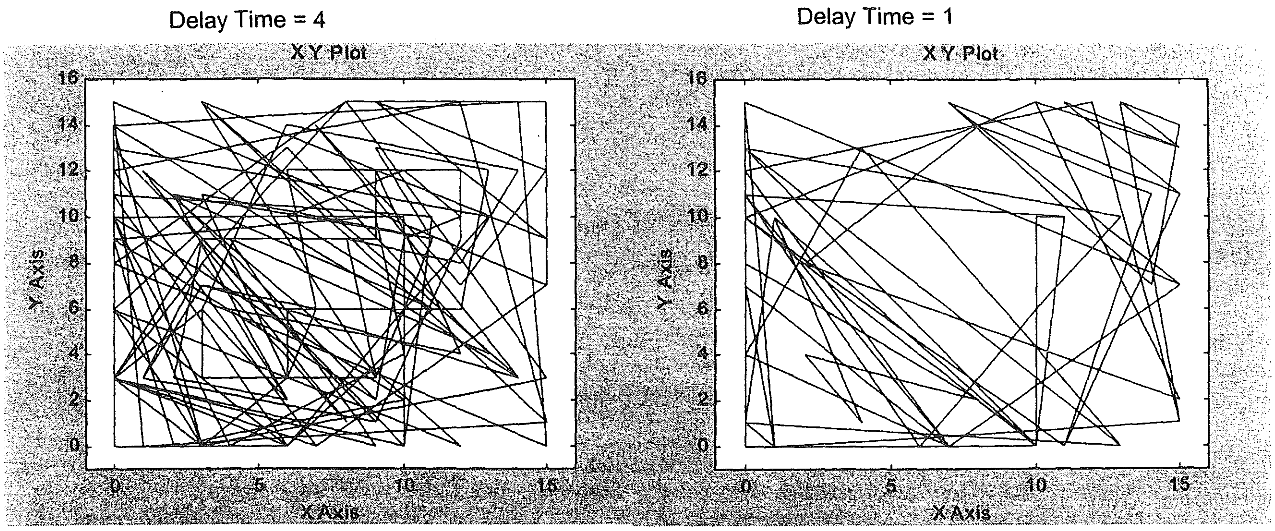


Figure 11.- Phase Diagram for different delay times.

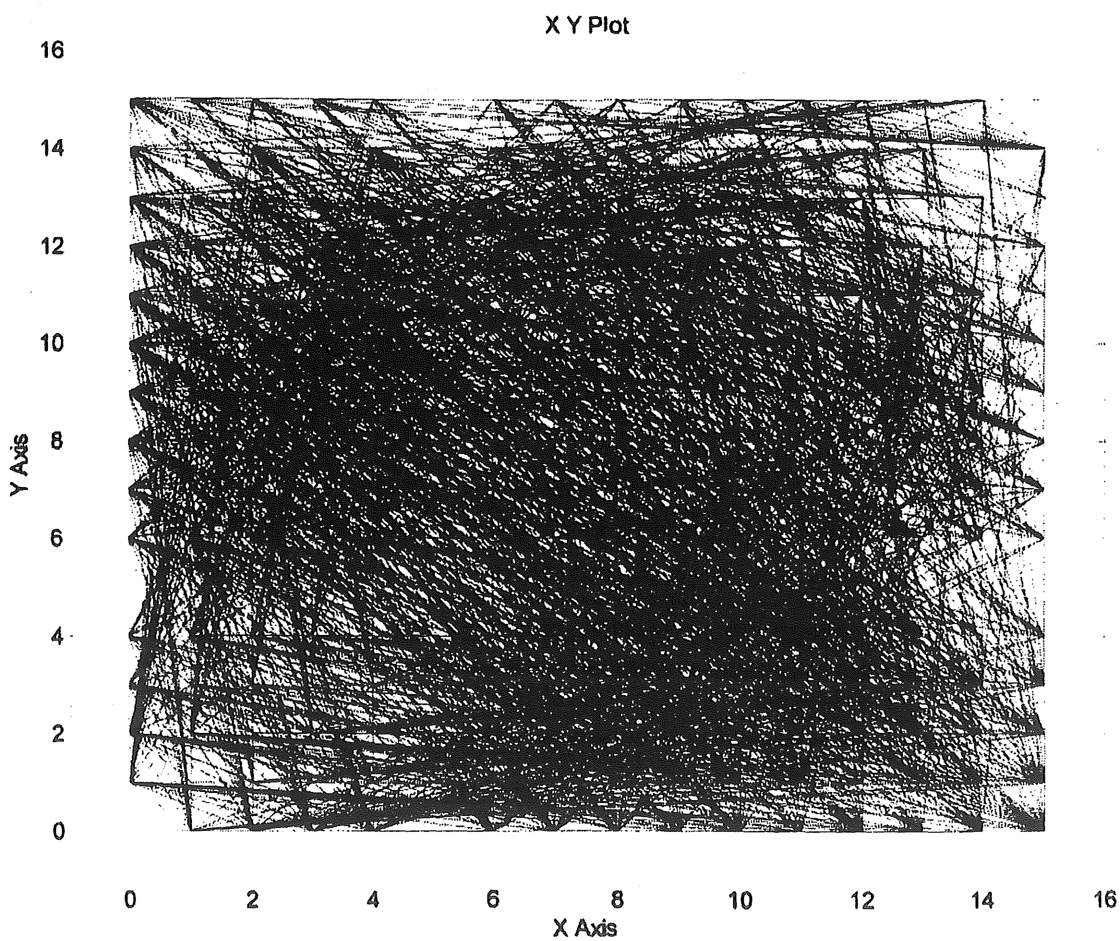


Figure 12.- Phase Diagram of Digital Chaos Signal.

been done in previous publications[3].

6. CONCLUSIONS

The reported results indicate at least two relevant conclusions. First, we can assure that when we can represent the characteristic function of a device as working diagram with properties of fractal geometry as the one we reported we could obtain some information about the device tolerance. The self-similarity dimension of a fractal structure can gives us information about the precision level that assure us the expected behaviour of the device.

Second, an easier analysis than with dimension can be done with the representations of phase diagram. As far as this diagram does not change, we can be sure there is not dependence with tolerance. Also, using the same technique of phase diagram we can evaluate the behaviour of the device on its dependence with the internal delay time or time device response.

Further, the presented method will indicate that some chaotic behaviour could be obtained from the device. In our case, the fractal structure has been demonstrated. The phase diagram indicates the dependence with precision level and internal delay time. A digital chaos signal has been obtained. Different application can be found for this device as the one presented in another paper of this Symposium[10].

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